Workshop on "Device Modeling and Circuit Simulation for Integrated Circuit Designs"

09 to 13 June 2025

Program Schedule:

Day	Time	Module* / Activity	Instructor / TA
1.	8:30 – 9:00am	Tea/ Coffee, Snacks	
	9:00 – 10:00am	**Introduction to the Course**	**Prof. Yash/Rutu**
	10:00 – 11:00am	**Introduction to VLSI**	**Prof. Rutu**
	11:00 – 11:15am	Break	
	11:15am – 12:15pm	**Introduction to Simulation and Modeling Analysis**	**Prof. Yash**
	12:15 – 1:15pm	**Introduction to SPICE Simulator**	**Prof. Yash / Rutu**
	1:15 – 2:15pm	Lunch Break	
	2:15 – 4:15pm	**Lab Exercise on SPICE Simulator for Circuit Implementation and Analysis**	**Prof. Yash/Rutu TA**
	4:15 – 4:30pm	Tea/coffee break	
	4:30 – 6:00pm	**Lab Exercise on Circuit design using BJTs and MOSFETs using SPICE**	**Prof. Yash/Rutu TA**
2.	8:30 – 9:00am	Tea/ Coffee, Snacks	
	9:00 – 10:00am	**Introduction to Digital Design**	**Prof. Rutu**
	10:00 – 11:00am	**Design Strategies for System Design**	**Prof. Rutu**
	11:00 – 11:15am	Break	
	11:15am – 12:15pm	**Introduction to Analytical Modeling of MOS Devices**	**Prof. Yash**
	12:15 – 1:15pm	**Parameter Extraction and Circuit Analysis**	**Prof. Yash**
	1:15 – 2:15pm	Lunch Break	
	2:15 – 4:15pm	**Lab Exercise 3 on MOS Device Modeling, Circuit Analysis and Parasitic Extraction**	**Prof Yash/Rutu TA**
	4:15 – 4:30pm	Tea/coffee break	
	4:30 – 6:00pm	**Lab Exercise 4 on some Digital System Design**	**Prof Yash/Rutu TA**

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3.	8:30 – 9:00am	Tea/ Coffee, Snacks	
	9:00 – 10:00am	**Introduction to Device Fabrication and Strategies**	**Prof. Yash**
	10:00 – 11:00am	**Analog Circuit Design-I**	**Prof. Rutu**
	11:00 – 11:15am	Break	
	11:15am – 12:15pm	**Analog Circuit Design-II**	**Prof. Rutu**
	12:15 – 1:15pm	**System Design-I**	**Prof. Yash/Rutu**
	1:15 – 2:15pm	Lunch Break	
	2:15 – 4:15pm	**Lab Exercise on System Design-I**	**Prof Yash/Rutu TA**
	4:15 – 4:30pm	Tea/coffee break	
	4:30 – 6:00pm	**Lab exercise on System Design-II**	**Prof Yash/Rutu TA**
4.	8:30 – 9:00am	Tea/ Coffee, Snacks	
	9:00 – 10:00am	**Introduction to Interconnects, 3D-ICS, NoC and SoC**	**Prof. Yash**
	10:00 – 11:00am	**System Design-II**	**Prof. Rutu**
	11:00 – 11:15am	Break	
	11:15am – 12:15pm	**Introduction to Memory Structures**	**Prof. Rutu**
	12:15 – 1:15pm	**Layout and Design Implementation**	**Prof. Yash**
	1:15 – 2:15pm	Lunch Break	
	2:15 – 4:15pm	**Lab Exercise on Interconnect Modeling and Analysis**	**Prof Yash/Rutu, TA**
	4:15 – 4:30pm	Tea/coffee break	
	4:30 – 6:00pm	**Lab Exercise on Layout**	**Prof Yash/Rutu, TA**
Day	**Time**	**Module* / Activity**	**Instructor / TA**
	8:30 – 9:00am	Tea/ Coffee, Snacks	
	9:00 – 10:00am	**Introduction to Next-Generation Devices and Interconnects**	**Prof. Yash**
	10:00 – 11:00am	**Nanoelectronics – The Futuristic Era**	**Prof. Rutu**

5.	11:00 – 11:15am	Break	
	11:15am – 12:15pm	**Simulation and Analysis of Advanced SET and GNRFET structures**	**Prof Yash/Rutu**
	12:15 – 1:15pm	**Prospective Research Area and Future Trends**	**Prof. Yash/Rutu**
	1:15 – 2:15pm	Lunch Break	
	2:15 – 4:15pm	**Lab Exercise on System Design and Analysis**	**Prof Yash/Rutu TA**
	4:15 – 4:30pm	Tea/coffee break	
	4:30 – 6:00pm	**Lab Exercise on System Design and Analysis**	**Prof Yash/Rutu TA**