Workshop on "Speech and Audio Signal Processing using FPGA"

16 to 20 June 2025

Program Schedule:

Day and Date	Time	Module/Activity	Instructor/TA
Day 1 Date: 16th June 2025	Lecture (9:00 am to 11:00 am)	Introduction to Speech and Audio Processing, Speech Applications, Speech Communication Pathway, Speech Production Modeling using LTI systems. Design of 2nd order digital resonators	Prof. Hemant A. Patil
	Lecture (11:00 AM to 1:00 PM)	Introduction to Hardware Description language for System Design	Prof. Yash Agrawal
	Lab (2:00 PM to 4:00 PM)	Hands-on-training on HDL-Verilog Simulator, Analyzing input output signals on Verilog	Prof. Yash Agrawal & TAs
	Lab (4:00 PM to 6:00 PM)	Introduction to MATLAB Programming, Writing Functions, Display of Speech and Audio/Music/Image/Video Signals, MATLAB Implementation of 2nd order digital resonaotrs	Prof. Hemant A. Patil & TAs
Day 2 Date: 17th June 2025	Lecture (9:00 AM to 11:00 AM)	Continuous-Time Fourier transform (CTFT), Discrete Fourier Transform (DFT) and hardware efficient implement of DFT via Fast Fourier Transform, Radix-2 FFT architecture.	Prof. Hemant A. Patil
	Lecture (11:00 AM to 1:00 PM)	Realization of Combinational and Sequential circuit designs for DFT, FFT architectures using Verilog HDL	Prof. Yash Agrawal
	Lab (2:00 PM to 6:00 PM)	Designing and realization of basic building blocks for DFT, FFT architectures on Verilog HDL	Prof. Yash Agrawal & TAs
	Lab (4:00 PM to 6:00 PM)	Plot of Magnitude Spectrum and Phase spectrum of speech signal Significance of Phase in Speech, Audio, and Image Processing Applications	Prof. Hemant A. Patil & TAs
Day 3 Date: 18th June 2025	Lecture (9:00 AM to 11:00 AM)	Short-time Fourier Transform (STFT) , wideband *vs* narrowband spectrograms	Prof. Hemant A. Patil
	Lecture (11:00 AM to1:00 PM)	Hardware designs for Audio Processing	Prof. Yash Agrawal
	Lab (2:00 PM to 6:00 PM)	Hands-on-training on Audio Processing using Verilog HDL	Prof. Yash Agrawal & TAs
	Lab (4:00 PM to 6:00 PM)	Spectrographic analysis for a case study on infant cry for normal *vs.* pathological infant cries	Prof. Hemant A. Patil & TAs

		Writing MATLAB code for (narrowband *vs.* wideband) spectrogram of speech and audio signals	
Day 4 Date: 19th June 2025	Lecture (9:00 AM to 11:00 AM)	Sampling and Quantization, Motivation for sampling (ability to delay the signal in discrete-time domain, ability to achieve cost effective narrowband (-3 dB BW) filters), Shannon's sampling paradigm: Pre- (anti-aliasing) filter, impulse-train sampler, and post filter Key issue in hardware: Difficulty in transmitting large amplitude and narrow impulses => avoid it using Zero-Order Hold (ZOH) and hence, design of Sample and Hold Circuit Brief introduction to frame concept for noise reduction, oversampling and design of sigma-delta Analog to Digital Converter (ADC) circuit.	Prof. Hemant A. Patil
	Lecture (11:00 AM to 1:00 PM)	Introduction of FPGA Embedded Board and design fundamentals	Prof. Yash Agrawal
	Lab (2:00 PM to 4:00 PM)	System design using FPGAs Implementation of ADC using circuit/gate level design	Prof. Yash Agrawal & TAs
	Lab (4:00 PM to 6:00 PM)	Effect of Undersampling: Stroboscopic Effect, Movies Implementation of Sample and Hold Circuit Implementation of Sigma-Delta ADC	Prof. Hemant A. Patil & TAs
Day 5 Date: 20th June 2025	Lecture (9:00 AM to 11:00 am)	Mel Frequency Cepstral Coefficients (MFCC) Constant Q Transform (CQT) and applications to Speech, Audio, and Music Processing	Prof. Hemant A. Patil
	Lecture (11:00 AM to 1:00 PM)	IP and SoC based System Realization for Audio Processing using FPGA Exposure to NN based System Realization for DSP using Excel and FPGA	Prof. Yash Agrawal
	Lab (2:00 PM to 6:00 PM)	Hardware Accelerators for Audio Processing using FPGA	Prof. Yash Agrawal & TAs
	Lab (4:00 PM to 6:00 PM)	MATLAB Implementations for MFCC and CQCC	Prof. Hemant A. Patil & TAs